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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,084	03/04/2002	Donald C. Soltis JR.	10016691-1	5905

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EXAMINER

COLEMAN, ERIC

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/091,084

Applicant(s)

SOLTIS ET AL.

Examiner

Eric Coleman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 March 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 5 comprises the language "processing...instructions... without being affected by the step of modifying". The scope meaning of this language is unclear (i.e., what element is not affected by the step of modifying?).

Claim Rejections - 35 USC § 103

3. Claims 1,3-7,10,19,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (patent no. 6,848,100).
4. Wu taught the invention substantially as claimed including a data processing ("DP") system comprising: method and processor for optimizing the processing of instructions through a processor (e.g., col. 1, lines 19-30 and col. 2, line 61-col. 3, line 28 and fig 11) comprising: processing like instructions through two or more instruction paths of the processor, each of the paths having different profile characteristics or heuristics (e.g., see col. 3, line 31-col. 4 line 9, and col. 7, lines 16-col. 8, line 11 and col. 13, line 1-col. 14, line 9); monitoring progress of the first like instructions through the instruction paths (e.g., see col. 3, line 31-col. 4, line 9, and col. 7, line 16-col. 8, line 11, and col. 13, line 1-col. 14, line 9).

5. Wu taught determining a profile value or path sum for each of the instruction paths in processing the first like instructions (e.g., see col. 8, lines 44-51, col. 12, line 55-col. 14, line 4). Wu did not expressly detail (claims 1) determining which of the paths is a first leader. However since an objective to the Wu system was to provide data for optimizing the processing of instructions along various paths by determining the path sum along various paths one of ordinary skill would have been motivated to use this data to determine the best path by merely comparing path sums. This would have provided a readily available means and method for using the teachings of Wu to reach one of its objectives of optimizing processing of instructions (e.g., see col. 1, lines 15-61 and col. 2, line 61-col. 3, line 4).

6. Wu did not expressly detail that the heuristics were altered (claims 1,3, 4, 7,10 19,20). Wu however taught modifying the path counts and profile of the instruction paths based on the path counts or profile values (this pertains to each path the therefore would have pertained to the each leader path) (col. 4, line 27-col. 7, line 54). Further (claim 10) as the processing would have different leaders during processing, the profile counts for each leader similarly would have been modified. Consequently, it would have been obvious to one of ordinary skill in the DP art that the heuristics of the paths would have to have been altered as Wu taught one objective of the heuristic could be to reduce added edges or reduce profiling overhead (e.g., see col. 14, line 46-col. 15, line 16). This would at times have provided different path counts for the various paths. Also since Wu taught an objective of the system was to improve optimizing the processing of instructions for various paths it would have been obvious to one of ordinary skill that

these Wu teachings would improve per thread performance. [Note the claims are broad enough to read on the situation where the heuristic of the leader are used to modify the heuristics of the leader and this situation is obvious in view of Wu as discussed above]. [As to limitation of the each parallel path having an array of pipeline pipelined execution units in the preamble of claim 19, this limitation is not necessary for the body of the claim to be complete, or referred to in the body of the claim, and therefore is not given any weight].

7. As per claim 5, to the extent claim 5 is understood, Wu taught selectively modifying the path counts for particular paths and therefore when the modifying was not selected for a particular path it would have been obvious to one of ordinary skill that the heuristic would have not have been modified (e.g., see col. 10, line 1-col. 12, line 52).

8. As per claim 6, Wu taught processing plural instructions through each path and did not teach executing the same instructions multiple times in the same path therefore with respect to process the same instructions there would have been not redundancy (e.g. see col. 12, lines 55-67).

9. Claims 2,8,9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu as applied to claims 1,19 above, and further in view of Cota-Robles (patent No. 6,658,447).

10. Cota-Robles taught grouping first like instructions as a bundle from common program thread (e.g., see col. 4. lines 12-37). One of ordinary skill would have been motivated to incorporate the Cota-Robles teachings of bundling instructions from plural threads to execute at least to provide for more efficient processing of instructions as the

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instruction slots for processing instructions concurrently would have been filled thereby maximizing the number of instructions processed per clock cycle (e.g., see col. 4, lines 38-65).

11. As per claims 8,9, Cota-Robles taught heuristics comprising tracking counts of cache misses for each thread, counts of unresolved branch instructions for each thread and counts of fetched and not yet issued or issued but not yet retired instructions (e.g., see col. 6, line 59-col. 7, line 15). One of ordinary skill in the DP art would have been motivated to combine the Cota-Robles teachings or particular heuristics for instruction processing at least to facilitate the use of the data generated by the Wu system in the providing of increase efficiency of instruction processing.

12. Claims 11,13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (patent no. 6,848,100) in view of Morikawa (patent No. 5,909,565).

13. Wu taught the invention substantially as claimed including a data processing ("DP") system comprising: method and processor for optimizing the processing of instructions through a processor (e.g., col. 1, lines 19-30 and col. 2, line 61-col. 3, line 28 and fig 11) comprising: processing like instructions through two or more instruction paths of the processor, each of the paths having different profile characteristics or heuristics (e.g., see col. 3, line 31-col. 4 line 9, and col. 7, lines 16-col. 8, line 11 and col. 13, lines 1-col. 14, line 9); monitoring progress of the first like instructions through the instruction paths (e.g., see col. 3, line 31-col. 4 line 9, and col. 7, lines 16-col. 8, line 11 and col. 13, lines 1-col. 14, line 9).

14. Wu taught determining a profile value or path sum for each of the instruction paths in processing the first like instructions (e.g., see col. 8, lines 44-51, col. 12, line 55-col. 14, line 4). Wu did not expressly detail (claims 1) determining which of the paths is a first leader. However since an objective to the Wu system was to provide data for optimizing the processing of instructions along various paths by determining the path sum along various paths one of ordinary skill would have been motivated to use this data to determine the best path by merely comparing path sums. This would have provided a readily available means and method for using the teachings of Wu to reach one of its objectives of optimizing processing of instructions (e.g., see col. 1, lines 15-61 and col. 2, line 61-col. 3, line 4).

15. Wu did not expressly detail that the heuristics were altered (claims 11,14,16). Wu however taught modifying the path counts and profile of the instruction paths based on the path counts or profile values (this pertains to each path the therefore would have pertained to the each leader path) (col. 4, line 27-col. 7, line 54). Further as the processing would have different leaders during processing, the profile counts for each leader similarly would have been modified. Consequently, it would have been obvious to one of ordinary skill in the DP art that the heuristics of the paths would have to have been altered as Wu taught one objective of the heuristic could be to reduce added edges or reduce profiling overhead (e.g., see col. 14, line 46-col. 15, line 16). This would at times have provided different path counts for the various paths. Also since Wu taught an objective of the system was to improve optimizing the processing of instructions for various paths it would have been obvious to one of ordinary skill that this

Wu teachings would improve per thread performance. [Note the claims are broad enough to read on the situation where the heuristic of the leader are used to modify the heuristics of the leader and this situation is obvious in view of Wu as discussed above].

16. As to the limitations of claim 15, one of ordinary skill would have been motivated to process various types of instruction through a profiling system such as taught by Wu at least to determine how each type of instruction or thread of instructions would operate and what system resources would be required so that processing of instructions would be optimized as was an objective to the Wu system as discussed above.

17. Wu did not expressly detail (claim 11) that each of the paths having an array of pipeline execution units. Morikawa however taught plural paths in a processor each path with an array of pipeline processing units (e.g., see fig.1).

18. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Wu and Morikawa. Wu taught the system comprised any process or capable of augmenting control flow graphs comprising a personal computer, mainframe, handheld device, portable computer, set-top box or any other system that includes software (e.g., see col. 15, lines 8-17). Consequently one of ordinary skill would have been motivated to use a system that would have efficiently augmented control flow graphs and Morikawa provided system with plural pipelines with each comprising plural processors (e.g., see fig. 1) and therefore one of ordinary skill would have motivated to implement the teachings of Wu using the Morikawa system. Also Morikawa taught (claim 13) a system that one of ordinary skill would have been motivated to implement

on a single die to provide for a cheaper system with faster transfer of data/instructions between the processor and coprocessor (e.g., see fig. 1).

19. Claims 12,17,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu and Morikawa as applied to claims 11 above, and further in view of Cota-Robles (patent No. 6,658,447).

20. Cota-Robles taught (claim 17,18) grouping first like instructions as a bundle from common program thread (e.g., see col. 4. lines 12-37). One of ordinary skill would have been motivated to incorporate the Cota-Robles teachings of bundling instructions from plural threads to execute at least to provide for more efficient processing of instructions as the instruction slots for processing instructions concurrently would have been filled thereby maximizing the number of instructions processed per clock cycle (e.g., see col. 4, lines 38-65).

21. As per claims 12 Cota-Robles taught heuristics comprising tracking counts of cache misses for each thread, counts of unresolved branch instructions for each thread and counts of fetched and not yet issued or issued but not yet retired instructions (e.g., see col. 6, lines 59-col. 7, line 15). One of ordinary skill in the DP art would have been motivated to combine the Cota-Robles teachings or particular heuristics for instruction processing at least to facilitate the use of the data generated by the Wu system in the providing of increase efficiency of instruction processing.

22. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tarsy (patent No. 5,367,687) disclosed a method and apparatus for optimizing cost-based heuristic instruction scheduling (e.g., see abstract).

Ravichandran (patent No. 5,966,537) disclosed a method and apparatus for dynamically optimizing an executable computer program using input data (e.g., see abstract).

Moona (patent No. 6,856,951) disclosed a system for repartitioning performance estimation in a hardware-software system (e.g., see abstract).

Chow (patent No. 6,128,775) disclosed a system for performing register promotion via load and store placement optimization with an optimizing compiler (e.g., see abstract).

Lu (patent No. 6,810,094) disclosed a viterbi decoder with pipelined parallel architecture with a branch metrics unit and best path unit (e.g., see abstract).

Schepers (patent No. 5,712,996) disclosed a process for dividing instructions of a computer program into instruction groups for parallel processing (e.g., see abstract).


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC



ERIC COLEMAN
PRIMARY EXAMINER